

Final Exam Review ECE 429/629 Fall 2003

The final exam will be open-book, open-notes.

Exam will consist of

- Short answer questions (Sections 3.1-3.11, 4.1, some of 4.4-4.5, 5.1-5.2)
- dynamic branch prediction question (Section 3.4)
- loop unrolling question (Section 4.1)
- cache memory question (Sections 5.1 and 5.2)

Thus, students should

- be familiar with the details of Sections 3.4, 4.1, 5.1, and 5.2 of the textbook
- have at least a cursory knowledge (for the short answer questions) of 3.1-3.11, 4.1, 5.1-5.2, and some of 4.4-4.5 (SW pipelining, trace scheduling, predicated instructions)
- not need to resort to the *COD* book (unless you simply want a readable introduction to the cache material that is in the course textbook)

For the exam, students should be able to

- explain the difference between a reservation station (RS) and a reorder buffer (ROB)
- define the following terms: speculation, predicated instruction, multiple issue, thread-level parallelism, trace scheduling, translation lookaside buffer (TLB)
- explain the primary limitation of a 1-bit branch predictor
- identify the relationship between software pipelining and Tomasulo's algorithm
- describe the differences between a branch prediction buffer, a two-bit predictor, a correlating branch predictor, a branch target buffer, a return address predictor, and a tournament predictor
- list the two primary flavors of multiple issue machines (superscalar and VLIW)
- give examples of superscalar, VLIW, and EPIC machines
- match the concepts of dynamic and static scheduling with the application areas of desktop, server, and embedded systems
- explain the benefits of allowing just two instructions to issue each clock cycle, one integer and one floating point
- match the Pentium machines with the P5, P6, and NetBurst microarchitectures
- walk through the states of a 2-bit branch predictor
- unroll a loop in assembly
- explain the difference between write-back and write-through cache
- map a virtual address to a physical address
- list the contents of a direct-mapped (or set-associative or fully associative) cache after each memory access

Sample short answer questions:

- Match the following computers (Pentium, Pentium Pro, PII, PIII, P4) with the following microarchitectures (P5, P6, NetBurst)

- List at least one goal achieved by each of the following: reservation station (RS) and reorder buffer (ROB)
- Does virtual memory generally use a write-back or a write-through cache? Why?
- Give an example of a system you could buy today in each of the following categories: superscalar, VLIW, and EPIC.
- How does multiple-issue affect CPI? What is the motivation behind implementing multiple issue with the restriction of one integer instruction and one floating-point instruction?
- Match the concepts of dynamic and static scheduling with the application areas of desktop, server, and embedded systems
- What is a predicated instruction? What effect does it have on dependences?
- What is speculative execution? What is the connection between speculation and a reorder buffer (ROB)?
- List the following in increasing order of performance: a tournament predictor, a branch prediction buffer, a two-bit predictor, a 1-bit predictor, and a correlating branch predictor
- What is a translation lookaside buffer (TLB), and what problem is it designed to overcome?
- What is trace scheduling? Would trace scheduling be more useful on a single-issue machine or a multiple-issue machine?
- What is thread-level parallelism?